Response to Rejection of Claims 1-25 Under 35 U.S.C. § 103(a)

The Examiner asserts that Javanifard discloses a circuit comprising a reference circuit, a voltage regulator electrically coupled to the reference circuit which generates a first control signal, and a charge pump that receives the control signal and generates a test supply voltage. Therefore, the Examiner asserts that Javanifard shows all elements of Claim 1 except for the reference circuit having a plurality of voltage regulation devices and having at least one bypass device connected to at least one of the plurality of voltage regulation devices. Furthermore, the Examiner states that Figure 5 of Furumochi shows "a reference circuit having a plurality of voltage regulation devices and at least one bypass device connected to at least one of the plurality of voltage regulation devices." The Examiner also states that "it would have been obvious to one having ordinary skill in the art to use Furumochi's figure for Javanifrad et al.'s reference circuit for the purpose of generating a variable reference voltage, therefore controlling the output level of the charge pump." Moreover, the Examiner states that with the combination, it is inherent that the at least one bypass device is activated following the certification of the semiconductor device to bypass the at least one of the plurality of voltage regulation devices from the clamp circuit to lower the clamping threshold of the clamp circuit, the voltage regulator generating a second control signal responsive to the lowered clamping threshold of the clamp circuit to cause the charge pump to generate the operational supply voltage. For the reasons set forth below, Applicants respectfully disagree.

Claims 1, 4, 15 and 25

Applicants respectfully submit that the Examiner has not established a *prima facie* case of obviousness as to Claim 1 because: (1) the cited references, individually or in combination, do not teach or suggest every feature of Claim 1; and (2) there is no suggestion or motivation to combine or modify the cited references in a way that would make Claim 1 obvious in view of the prior art.

Claim 1 of the present invention is directed to a voltage control circuit comprising, among other elements, a clamp circuit having a plurality of voltage regulation devices that

control a clamping threshold of the clamp circuit. The term "clamp circuit," as would be understood by one with ordinary skill in the relevant art, describes a circuit that operates to place a limit on (or to clamp) a signal if the signal reaches a certain predetermined value. This limiting, or clamping, does not occur until the signal reaches the predetermined value, and the signal is allowed to vary until that point. This understanding of the term "clamp circuit" is also supported by the surrounding claim language of Claim 1. Claim 1 recites this limit controlled by the clamp circuit as the "clamping threshold." As appreciated by one with ordinary skill in the relevant art, and consistent with the understanding of a clamp circuit, the term "clamping threshold" corresponds to a limit placed on a signal wherein some action occurs when the signal reaches that limit. Thus, the clamp circuit of Claim 1 operates to place a limit on a signal when that signal reaches a certain predetermined level. This limit on the voltage signal corresponds to the clamping threshold of the clamp circuit and ensures that the safe operating voltage of the charge pump is not exceeded.

Neither Javanifard nor Furumochi teaches or suggests a voltage control circuit comprising a clamp circuit having a clamping threshold. Javanifard discloses a circuit for generating a desired output voltage (see column 19, line 16). With reference to Figure 14, Javanifard shows a supply circuit having, among other elements, a reference circuit. This voltage reference circuit is disclosed as using an input voltage to generate a reference voltage. Nowhere in the specification or in the depicted embodiments does Javanifard teach or suggest a voltage control circuit having a clamp circuit or a circuit having a clamping threshold. In particular, the reference voltage is fixed such that it does not vary above or below the desired voltage.

Like Javanifard, Furumochi does not teach or suggest a voltage control circuit having a clamp circuit. Furumochi describes in column 2 at lines 59-60 that its invention relates to a voltage generator circuit for generating "constant voltages in fine steps." Referring to the preferred embodiment of the invention depicted in Figure 5, Furumochi describes the constant voltage generator as being designed for supplying a constant voltage with "strict precision" (see column 7, lines 16-17). The voltage supplied by the Furumochi circuit is kept fixed, as noted by

the Examiner, and is not allowed to vary above or below the voltage selected by the diode-configured transistors that are not bypassed. To assert that Furumochi teaches or suggests a clamp circuit not only goes against the accepted meaning of the term, but also ignores other express limitations of Claim 1, including the limitation of a "clamping threshold." Furumochi does not teach a circuit that allows an output signal to vary up to a clamping threshold. Rather, once the selected diode-configured transistors are bypassed in Furumochi, the output signal is fixed and does not vary above or below the selected output voltage. Thus, Furumochi, in combination with Javanifard, does not render obvious the embodiment of the present invention recited in Claim 1, which includes a clamp circuit having a clamping threshold. See M.P.E.P. § 2143.03 (all words in claim must be considered in judging the patentability of that claim against prior art).

In addition to reciting a voltage control circuit having a clamp circuit, Claim 1 of the present invention also recites the voltage control circuit having at least one bypass device that is activated following certification of the semiconductor device to bypass at least one of a plurality of voltage regulation devices from the clamp circuit to lower the clamping threshold of the clamp circuit. This lower clamping threshold limits the supply voltage of the semiconductor device and prevents the customer from subsequently testing the semiconductor device using harmful voltage levels.

Neither Javanifard nor Furumochi recites a voltage control circuit that comprises a bypass device that is activated following the certification of a semiconductor device to bypass at least one of a plurality of voltage regulation devices to lower the clamping threshold of a clamp circuit. Rather, Furumochi discloses a constant voltage generator having a switching element (SW0) comprising an n-type transistor connected at its gate to a ROM fuse circuit via an inverter (see column 7, lines 45-50). This switching element, however, cannot be activated to bypass a voltage regulation device in order to lower a clamping threshold. Specifically, the switching element taught by Furumochi may operate either in an "ON" state or an "OFF" state. When in an "ON" state, the switching element bypasses a transistor T4 and causes the output voltage of

the voltage generator circuit be at a lower level. When in an "OFF" state, the switching element does not bypass transistor T4 and causes the output voltage of the voltage regulator to be at a higher level (see Table 1). However, the switching element disclosed by Furumochi may not "switch" from the "OFF" state (higher output voltage) to the "ON" state (lower output voltage). This is because, to be in the "OFF" state, fuse elements of the ROM fuse circuit in the switching element are melted and disconnected (see, for example, column 9, lines 22-33). In other words, the "OFF" state, which results in a higher output voltage produced by the voltage generator circuit, is permanent, and the switching element cannot subsequently be activated (or switched to an "ON" state) to lower the output voltage of the voltage generator circuit. Thus, neither of the cited references discloses a bypass device that may be activated to lower the clamping threshold of a clamp circuit.

Furthermore, there is no suggestion or motivation to combine or to modify the references that would make Claim 1 of the present invention obvious to one of ordinary skill in the art. Javanifard and Furumochi, individually or in combination, teach away from the claimed invention. Both Figure 14 of Javanifard and Figure 5 of Furumochi disclose reference circuits. In particular, the reference circuit disclosed in Furumochi is designed to generate a fixed reference voltage. Such a high precision reference circuit for producing a fixed reference voltage teaches away from the use of a clamp circuit that allows an output signal to vary below a clamping threshold. Because Furumochi teaches away from the present invention, Applicants submit that there is no suggestion or motivation to combine Javanifard and Furumochi in a way to render the present invention obvious.

Independent Claims 4, 15 and 25 are believed to be patentable for the reasons set forth above and for the different features recited therein.

Because Claims 1, 4, 15 and 25 include elements not taught or suggested by Javanifard or Furumochi, Applicants respectfully request the Examiner to withdraw the rejection of Claims 1, 4, 15, and 25 under 35 U.S.C. § 103(a) and to pass Claims 1, 4, 15 and 25 to allowance.

Claim 10

Claim 10 recites a voltage control circuit comprising, among other elements, means for controlling an output of a clamp circuit. As previously discussed, neither Javanifard nor Furumochi disclose a voltage control circuit having a clamp circuit. Thus, Applicants respectfully submit that Claim 10 is patentably distinguished over the cited references. Applicants respectfully request the Examiner to withdraw the rejection of Claim 10 and to pass Claim 10 to allowance.

Claim 17

Claim 17 recites a method of providing a first voltage supply on a semiconductor device during a first period and a second supply voltage during a second period. This method comprises, among other steps, generating the first supply voltage from a first voltage control signal, reversibly bypassing at least one of a plurality of voltage control elements, and generating the second supply voltage from a second voltage control signal that is established from the plurality of voltage control elements which are not reversibly bypassed.

Furumochi does not teach or suggest a method comprising the step of reversibly bypassing at least one of a plurality of voltage control elements. Rather, Furumochi discloses a switching element (SW0) wherein the gate of a transistor is connected to a ROM fuse circuit (see, for example, column 7, lines 45-50). In particular, the ROM fuse circuit of Furumochi comprises a resistor and a fuse element connected in series between a power source and a ground line (see column 8, lines 19-24). As previously discussed with respect to Claim 1, the "OFF" state of switching element SW0 is permanent because the fuse elements of the ROM fuse circuit are melted and disconnected to make the state "concrete" (see, for example, column 9, lines 22-33). Thus, the "OFF" state of the switching element SW0 is not reversible, and the switching element cannot reversibly bypass a voltage control element in order to establish a second voltage control signal. Nowhere does Furumochi teach or suggest the step of reversibly bypassing at least one of the plurality of voltage control elements.

Because Claim 17 includes elements not taught or suggested by Javanifard or Furumochi, Applicants respectfully request the Examiner to withdraw the rejection of Claim 17 under 35 U.S.C. § 103(a) and to pass Claim 17 to allowance.

Claims 2-3, 5-9, 11-14, 16 and 18-24

Claims 2-3 and 6-9 depend from Claim 1 and further define the invention defined in Claim 1. Claim 5 depends from Claim 4 and further defines the invention defined in Claim 4. Claims 11-14 depend from Claim 10 and further define the invention defined in Claim 10. Claim 16 depends from Claim 15 and further defines the invention defined in Claim 15. Claims 18-24 depend from Claim 17 and further define the invention defined in Claim 17. In view of the foregoing remarks regarding the patentability of Claims 1, 4, 10, 15, 17 and 25, Applicants respectfully submit that dependent Claims 2-3, 5-9, 11-14, 16 and 18-24 are also patentable. Applicants respectfully request the Examiner to withdraw the rejection under 35 U.S.C. § 103(a) of Claims 2-3, 5-9, 11-14, 16 and 18-24 to pass Claims 2-3, 5-9, 11-14, 16 and 18-24 to allowance.

Response to Examiner's Response to Applicants' Prior Arguments

On pages 4-5 of the May 31, 2002 Final Office Action, the Examiner states that Applicants' arguments submitted in response to the previous Office Action have been fully considered but are not persuasive. In particular, and in response to the Applicants' argument that the cited references do not teach a clamp circuit, the Examiner states:

> [I]t is well known that diode works as a clamp. The diodes in Furumochi's circuits forcing the output node to a fix voltage. Therefore, Furumochi's reference circuit can be considered as clamp circuits. . . . Furthermore, it is seen as inherent for the supply voltage to be vary. That why the diodes is used in the circuit for the purpose of generating a fix reference voltage when the supply voltage exceed the threshold voltages of the diodes.

Applicants agree with the Examiner that, under certain conditions, a diode may work as a clamping device. However, it is well known to one of ordinary skill in the relevant art that a

circuit containing a diode, or other clamping device, is not necessarily a clamp circuit. As set forth above, neither Furumochi nor Javanifard teaches or suggests the use of a clamping circuit. Even though Furumochi discloses the use of diode-configured transistors in its voltage reference circuit depicted in Figure 5, Furumochi never discloses or suggests a clamp circuit having a clamping threshold.

As discussed above, the "high-precision" voltage reference circuit of Furumochi teaches away from the claimed invention, which comprises a clamping circuit that allows an output voltage to vary up to a clamping threshold. If the reference circuit of Furumochi were designed to function as a clamping circuit with a clamping threshold, as the Examiner's statement suggests, the reference circuit of Furumochi would be rendered unsatisfactory for its intended purpose of supplying a "high precision" constant reference voltage. Such a modification of Furumochi's disclosure is improper and is not sufficient to establish a *prima facie* case of obviousness. See M.P.E.P. § 2143.01 (proposed modification cannot render prior art unsatisfactory for its intended purpose and cannot change the principal of operation of the prior art invention); See also *In re Gordon*, 733 F.2d 900, 902, 211 U.S.P.Q. 1125, 1127 (Fed. Cir. 1984); *In re Ratti*, 270 F.2d 810, 813, 123 U.S.P.Q. 349, 352 (C.C.P.A. 1959).

The Examiner also asserts in the last paragraph on page 5 that:

> In response for the arguments of claim 17, Furumochi's figure 4 shows the step of generating the first supply voltage (Vout when switch 11A opened) from the first control signal and reversibly bypassing at least one of the plurality of the voltage control elements (by switch 11A) which are not reversibly bypass, a second supply voltage (Vout when switch 11a closed) from the second control signal.

Applicants note that Figure 4 does not show a switch 11A, and Applicants assume that the Examiner's statement is intended to be directed to Figure 3 on the same page. Applicants also respectfully submit, in light of the remarks made above, that Furumochi's Figure 3 does not teach the step of reversibly bypassing at least one of a plurality of voltage control elements in order to establish a second voltage control signal. The Examiner's statement appears to be reading an element into Figure 3 that is not disclosed by Furumochi. When reading Figure 3

with the corresponding specification and subsequent figures, one with ordinary skill in the relevant art would understand the switching 11A of Figure 3 to be controlled by the ROM fuse circuit. Once the switching element 11A is opened (to not bypass transistor Tn), the switching element may not subsequently be closed because the open, or "OFF," state is permanent due to the configuration of the ROM fuse circuit. To open switching element 11A, Furumochi teaches that the fuse elements of the ROM fuse circuit are melted and disconnected, which creates an irreversible open state. Thus, Applicants submit that Figure 3, in view of the corresponding specification, does not disclose each step of Claim 17.

Summary

In view of the foregoing remarks, Applicants respectfully submit that Claims 1-25 are in condition for allowance, and Applicants respectfully request allowance of Claims 1-25. If there is any further impediment to the prompt allowance of this application, the Examiner is respectfully requested to call the undersigned attorney of record at 949-721-2849 or at the telephone number listed below.

Respectfully submitted,
KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: JULY 30, 2002

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